

## S9KEA128P80M48SF0

### KEA128 Sub-Family Data Sheet

Supports the following:

S9KEAZ64AMLK(R),  
S9KEAZ128AMLK(R),  
S9KEAZ64AVLK(R),  
S9KEAZ128AVLK(R),  
S9KEAZ64ACLK(R),  
S9KEAZ128ACLK(R),  
S9KEAZ64AMLH(R),  
S9KEAZ128AMLH(R),  
S9KEAZ64AVLH(R),  
S9KEAZ128AVLH(R),  
S9KEAZ64ACLH(R) and  
S9KEAZ128ACLH(R)

#### Key features

- Operating characteristics
  - Voltage range: 2.7 to 5.5 V
  - Flash write voltage range: 2.7 to 5.5 V
  - Temperature range (ambient): -40 to 125°C
- Performance
  - Up to 48 MHz ARM® Cortex-M0+ core
  - Single cycle 32-bit x 32-bit multiplier
  - Single cycle I/O access port
- Memories and memory interfaces
  - Up to 128 KB flash
  - Up to 16 KB RAM
- Clocks
  - Oscillator (OSC) - supports 32.768 kHz crystal or 4 MHz to 24 MHz crystal or ceramic resonator; choice of low power or high gain oscillators
  - Internal clock source (ICS) - internal FLL with internal or external reference, 37.5 kHz pre-trimmed internal reference for 48 MHz system clock
  - Internal 1 kHz low-power oscillator (LPO)
- System peripherals
  - Power management module (PMC) with three power modes: Run, Wait, Stop
  - Low-voltage detection (LVD) with reset or interrupt, selectable trip points
  - Watchdog with independent clock source (WDOG)
  - Programmable cyclic redundancy check module (CRC)
  - Serial wire debug interface (SWD)
  - Aliased SRAM bitband region (BIT-BAND)
  - Bit manipulation engine (BME)
- Security and integrity modules
  - 80-bit unique identification (ID) number per chip
- Human-machine interface
  - Up to 71 general-purpose input/output (GPIO)
  - Two 32-bit keyboard interrupt modules (KBI)
  - External interrupt (IRQ)
- Analog modules
  - One up to 16-channel 12-bit SAR ADC, operation in Stop mode, optional hardware trigger (ADC)
  - Two analog comparators containing a 6-bit DAC and programmable reference input (ACMP)

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

- Timers
  - One 6-channel FlexTimer/PWM (FTM)
  - Two 2-channel FlexTimer/PWM (FTM)
  - One 2-channel periodic interrupt timer (PIT)
  - One pulse width timer (PWT)
  - One real-time clock (RTC)
- Communication interfaces
  - Two SPI modules (SPI)
  - Up to three UART modules (UART)
  - Two I2C modules (I2C)
  - One MSCAN module (MSCAN)
- Package options
  - 80-pin LQFP
  - 64-pin LQFP

# Table of Contents

|       |   |    |       |  |    |
|-------|---|----|-------|--|----|
| 1     | Ordering parts.....                         | 4  | 4.2.2 | FTM module timing.....                                 | 16 |
| 1.1   | Determining valid orderable parts.....      | 4  | 4.3   | Thermal specifications.....                            | 17 |
| 2     | Part identification.....                    | 4  | 4.3.1 | Thermal characteristics.....                           | 17 |
| 2.1   | Description.....                            | 4  | 5     | Peripheral operating requirements and behaviors.....   | 19 |
| 2.2   | Format.....                                 | 4  | 5.1   | Core modules.....                                      | 19 |
| 2.3   | Fields.....                                 | 4  | 5.1.1 | SWD electricals .....                                  | 19 |
| 2.4   | Example.....                                | 5  | 5.2   | External oscillator (OSC) and ICS characteristics..... | 20 |
| 3     | Ratings.....                                | 5  | 5.3   | NVM specifications.....                                | 22 |
| 3.1   | Thermal handling ratings.....               | 5  | 5.4   | Analog.....  | 23 |
| 3.2   | Moisture handling ratings.....              | 5  | 5.4.1 | ADC characteristics.....                               | 23 |
| 3.3   | ESD handling ratings.....                   | 6  | 5.4.2 | Analog comparator (ACMP) electricals.....              | 25 |
| 3.4   | Voltage and current operating ratings.....  | 6  | 5.5   | Communication interfaces.....                          | 26 |
| 4     | General.....                                | 7  | 5.5.1 | SPI switching specifications.....                      | 26 |
| 4.1   | Nonswitching electrical specifications..... | 7  | 5.5.2 | MSCAN.....   | 29 |
| 4.1.1 | DC characteristics.....                     | 7  | 6     | Dimensions.....  | 29 |
| 4.1.2 | Supply current characteristics.....         | 13 | 6.1   | Obtaining package dimensions.....                      | 29 |
| 4.1.3 | EMC performance.....                        | 15 | 7     | Pinout.....  | 30 |
| 4.2   | Switching specifications.....               | 15 | 7.1   | Signal multiplexing and pin assignments.....           | 30 |
| 4.2.1 | Control timing.....                         | 15 | 8     | Revision History.....                                  | 30 |

# 1 Ordering parts

## 1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to [freescale.com](http://freescale.com) and perform a part number search for the following device numbers: KEAZ128.

# 2 Part identification

## 2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 2.2 Format

Part numbers for this device have the following format:

Q B KEA A C FFF M T PP N

## 2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

| Field | Description          | Values  |
|-------|----------------------|---|
| Q     | Qualification status | <ul style="list-style-type: none"> <li>S = Automotive qualified</li> <li>P = Prequalification</li> </ul>                    |
| B     | Memory type          | <ul style="list-style-type: none"> <li>9 = Flash</li> </ul>   |
| KEA   | Kinetis Auto family  | <ul style="list-style-type: none"> <li>KEA</li> </ul>   |
| A     | Key attribute        | <ul style="list-style-type: none"> <li>Z = M0+ core</li> <li>F = M4 W/ DSP &amp; FPU</li> <li>C = M4 W/ AP + FPU</li> </ul> |
| C     | CAN availability     | <ul style="list-style-type: none"> <li>N = CAN not available</li> <li>(Blank) = CAN available</li> </ul>                    |

*Table continues on the next page...*

| Field | Description               | Values  |
|-------|---------------------------|---|
| FFF   | Program flash memory size | <ul style="list-style-type: none"> <li>• 128 = 128 KB</li> </ul>  |
| M     | Maskset revision          | <ul style="list-style-type: none"> <li>• A = 1<sup>st</sup> Fab version</li> <li>• B = Revision after 1<sup>st</sup> version</li> </ul> |
| T     | Temperature range (°C)    | <ul style="list-style-type: none"> <li>• C = -40 to 85</li> <li>• V = -40 to 105</li> <li>• M = -40 to 125</li> </ul>                   |
| PP    | Package identifier        | <ul style="list-style-type: none"> <li>• LH = 64 LQFP (10 mm x 10 mm)</li> <li>• LK = 80 LQFP (14 mm x 14 mm)</li> </ul>                |
| N     | Packaging type            | <ul style="list-style-type: none"> <li>• R = Tape and reel</li> <li>• (Blank) = Trays</li> </ul>  |

## 2.4 Example

This is an example part number:

S9KEAZ128AMLK

## 3 Ratings

### 3.1 Thermal handling ratings

| Symbol           | Description                   | Min. | Max. | Unit | Notes |
|------------------|-------------------------------|------|------|------|-------|
| T <sub>STG</sub> | Storage temperature           | -55  | 150  | °C   | 1     |
| T <sub>SDR</sub> | Solder temperature, lead-free | —    | 260  | °C   | 2     |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

### 3.2 Moisture handling ratings

| Symbol | Description                | Min. | Max. | Unit | Notes |
|--------|----------------------------|------|------|------|-------|
| MSL    | Moisture sensitivity level | —    | 3    | —    | 1     |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

### 3.3 ESD handling ratings

| Symbol    | Description   | Min.  | Max.  | Unit | Notes |
|-----------|---|-------|-------|------|-------|
| $V_{HBM}$ | Electrostatic discharge voltage, human body model     | -6000 | +6000 | V    | 1     |
| $V_{CDM}$ | Electrostatic discharge voltage, charged-device model | -500  | +500  | V    | 2     |
| $I_{LAT}$ | Latch-up current at ambient temperature of °C         | -100  | +100  | mA   | 3     |

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78D, *IC Latch-up Test*. The test produced the following results:
  - Test was performed at 125 °C case temperature (Class II).
  - I/O pins pass +100/-100 mA I-test with  $I_{DD}$  current limit at 400 mA ( $V_{DD}$  collapsed during positive injection).
  - I/O pins pass +50/-100 mA I-test with  $I_{DD}$  current limit at 1000 mA for  $V_{DD}$ .
  - Supply groups pass 1.5  $V_{CCmax}$ .
  - RESET\_B pin was only tested with negative I-test due to product conditioning requirement.

### 3.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in the following table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either  $V_{SS}$  or  $V_{DD}$ ) or the programmable pullup resistor associated with the pin is enabled.

**Table 1. Voltage and current operating ratings**

| Symbol    | Description   | Min.           | Max.                        | Unit |
|-----------|---|----------------|-----------------------------|------|
| $V_{DD}$  | Digital supply voltage  | -0.3           | 6.0                         | V    |
| $I_{DD}$  | Maximum current into $V_{DD}$   | —              | 120                         | mA   |
| $V_{IN}$  | Input voltage except true open drain pins                                 | -0.3           | $V_{DD} + 0.3$ <sup>1</sup> | V    |
|           | Input voltage of true open drain pins                                     | -0.3           | 6                           | V    |
| $I_D$     | Instantaneous maximum current single pin limit (applies to all port pins) | -25            | 25                          | mA   |
| $V_{DDA}$ | Analog supply voltage   | $V_{DD} - 0.3$ | $V_{DD} + 0.3$              | V    |

1. Maximum rating of  $V_{DD}$  also applies to  $V_{IN}$ .

## 4 General

### 4.1 Nonswitching electrical specifications

#### 4.1.1 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

**Table 2. DC characteristics**

| Symbol           | Descriptions          |   | Min  | Typical <sup>1</sup>   | Max | Unit                     |
|------------------|-----------------------|---|--|------------------------|-----|--------------------------|
| —                | Operating voltage     |   | —  | 2.7                    | —   | 5.5 V                    |
| V <sub>OH</sub>  | Output high voltage   | All I/O pins, except PTA2 and PTA3, standard-drive strength | 5 V, I <sub>load</sub> = -5 mA                       | V <sub>DD</sub> - 0.8  | —   | — V                      |
|                  |                       |   | 3 V, I <sub>load</sub> = -2.5 mA                     | V <sub>DD</sub> - 0.8  | —   | — V                      |
|                  |                       | High current drive pins, high-drive strength <sup>2</sup>   | 5 V, I <sub>load</sub> = -20 mA                      | V <sub>DD</sub> - 0.8  | —   | — V                      |
|                  |                       |   | 3 V, I <sub>load</sub> = -10 mA                      | V <sub>DD</sub> - 0.8  | —   | — V                      |
| I <sub>OHT</sub> | Output high current   | Max total I <sub>OH</sub> for all ports                     | 5 V  | —                      | —   | -100 mA                  |
|                  |                       |   | 3 V  | —                      | —   | -60                      |
| V <sub>OL</sub>  | Output low voltage    | All I/O pins, standard-drive strength                       | 5 V, I <sub>load</sub> = 5 mA                        | —                      | —   | 0.8 V                    |
|                  |                       |   | 3 V, I <sub>load</sub> = 2.5 mA                      | —                      | —   | 0.8 V                    |
|                  |                       | High current drive pins, high-drive strength <sup>2</sup>   | 5 V, I <sub>load</sub> = 20 mA                       | —                      | —   | 0.8 V                    |
|                  |                       |   | 3 V, I <sub>load</sub> = 10 mA                       | —                      | —   | 0.8 V                    |
| I <sub>OLT</sub> | Output low current    | Max total I <sub>OL</sub> for all ports                     | 5 V  | —                      | —   | 100 mA                   |
|                  |                       |   | 3 V  | —                      | —   | 60                       |
| V <sub>IH</sub>  | Input high voltage    | All digital inputs  | 4.5 ≤ V <sub>DD</sub> < 5.5 V                        | 0.65 × V <sub>DD</sub> | —   | — V                      |
|                  |                       |   | 2.7 ≤ V <sub>DD</sub> < 4.5 V                        | 0.70 × V <sub>DD</sub> | —   | —                        |
| V <sub>IL</sub>  | Input low voltage     | All digital inputs  | 4.5 ≤ V <sub>DD</sub> < 5.5 V                        | —                      | —   | 0.35 × V <sub>DD</sub> V |
|                  |                       |   | 2.7 ≤ V <sub>DD</sub> < 4.5 V                        | —                      | —   | 0.30 × V <sub>DD</sub>   |
| V <sub>hys</sub> | Input hysteresis      | All digital inputs  | —  | 0.06 × V <sub>DD</sub> | —   | mV                       |
| I <sub>inl</sub> | Input leakage current | Per pin (pins in high impedance input mode)                 | V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub> | —                      | 0.1 | 1 μA                     |

Table continues on the next page...

**Table 2. DC characteristics (continued)**

| Symbol      | Descriptions                             |  |                                    | Min  | Typical <sup>1</sup> | Max  | Unit       |
|-------------|--|--|------------------------------------|------|----------------------|------|------------|
| $I_{INTOT}$ | Total leakage combined for all port pins | Pins in high impedance input mode  | $V_{IN} = V_{DD}$ or $V_{SS}$      | —    | —                    | 2    | $\mu A$    |
| $R_{PU}$    | Pullup resistors                         | All digital inputs, when enabled (all I/O pins other than PTA2 and PTA3) | —                                  | 30.0 | —                    | 50.0 | k $\Omega$ |
| $R_{PU}^3$  | Pullup resistors                         | PTA2 and PTA3 pins   | —                                  | 30.0 | —                    | 60.0 | k $\Omega$ |
| $I_{IC}$    | DC injection current <sup>4, 5, 6</sup>  | Single pin limit   | $V_{IN} < V_{SS}, V_{IN} > V_{DD}$ | -2   | —                    | 2    | mA         |
|             |  | Total MCU limit, includes sum of all stressed pins                       |                                    | -5   | —                    | 25   |            |
| $C_{in}$    | Input capacitance, all pins              |  | —                                  | —    | —                    | 7    | pF         |
| $V_{RAM}$   | RAM retention voltage                    |  | —                                  | 2.0  | —                    | —    | V          |

1. Typical values are measured at 25 °C. Characterized, not tested.
2. Only PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0, and PTH1 support high current output.
3. The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
4. All functional non-supply pins, except for PTA2 and PTA3, are internally clamped to  $V_{SS}$  and  $V_{DD}$ . PTA2 and PTA3 are true open drain I/O pins that are internally clamped to  $V_{SS}$ .
5. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger value.
6. Power supply must maintain regulation within operating  $V_{DD}$  range during instantaneous and operating maximum current conditions. If the positive injection current ( $V_{in} > V_{DD}$ ) is higher than  $I_{DD}$ , the injection current may flow out of  $V_{DD}$  and could result in external power supply going out of regulation. Ensure that external  $V_{DD}$  load will shunt current higher than maximum injection current when the MCU is not consuming power, such as when no system clock is present, or clock rate is very low (which would reduce overall power consumption).

**Table 3. LVD and POR specification**

| Symbol      | Description   |                             | Min | Typ  | Max | Unit |
|-------------|---|-----------------------------|-----|------|-----|------|
| $V_{POR}$   | POR re-arm voltage <sup>1</sup>   |                             | 1.5 | 1.75 | 2.0 | V    |
| $V_{LVDH}$  | Falling low-voltage detect threshold—high range (LVDV = 1) <sup>2</sup> |                             | 4.2 | 4.3  | 4.4 | V    |
| $V_{LVW1H}$ | Falling low-voltage warning threshold— high range                       | Level 1 falling (LVWV = 00) | 4.3 | 4.4  | 4.5 | V    |
| $V_{LVW2H}$ |   | Level 2 falling (LVWV = 01) | 4.5 | 4.5  | 4.6 | V    |
| $V_{LVW3H}$ |   | Level 3 falling (LVWV = 10) | 4.6 | 4.6  | 4.7 | V    |
| $V_{LVW4H}$ |   | Level 4 falling (LVWV = 11) | 4.7 | 4.7  | 4.8 | V    |
| $V_{HYSH}$  | High range low-voltage detect/ warning hysteresis                       |                             | —   | 100  | —   | mV   |

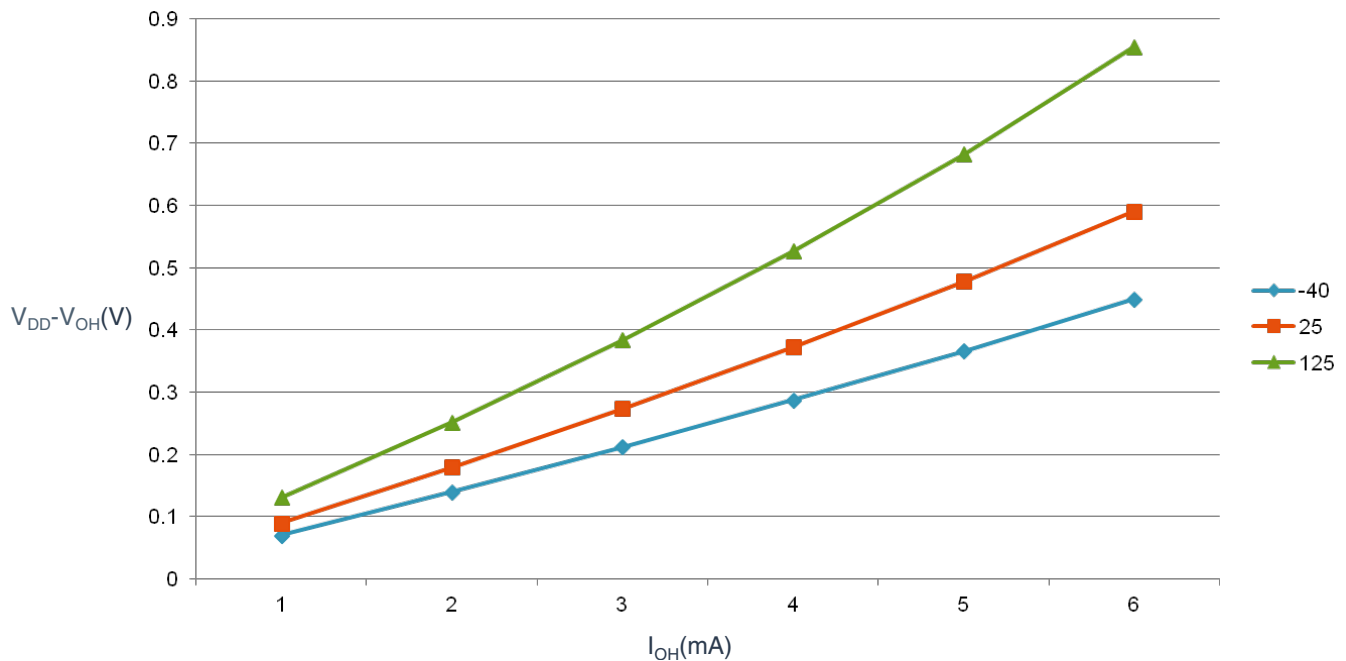
Table continues on the next page...



**Table 3. LVD and POR specification (continued)**

| Symbol              | Description   | Min                         | Typ  | Max  | Unit |   |
|---------------------|---|-----------------------------|------|------|------|---|
| V <sub>LVDL</sub>   | Falling low-voltage detect threshold—low range (LVDV = 0) | 2.56                        | 2.61 | 2.66 | V    |   |
| V <sub>LVW1L</sub>  | Falling low-voltage warning threshold—low range           | Level 1 falling (LVWV = 00) | 2.62 | 2.7  | 2.78 | V |
| V <sub>LVW2L</sub>  |   | Level 2 falling (LVWV = 01) | 2.72 | 2.8  | 2.88 | V |
| V <sub>LVW3L</sub>  |   | Level 3 falling (LVWV = 10) | 2.82 | 2.9  | 2.98 | V |
| V <sub>LVW4L</sub>  |   | Level 4 falling (LVWV = 11) | 2.92 | 3.0  | 3.08 | V |
| V <sub>HYS DL</sub> | Low range low-voltage detect hysteresis                   | —                           | 40   | —    | mV   |   |
| V <sub>HYS WL</sub> | Low range low-voltage warning hysteresis                  | —                           | 80   | —    | mV   |   |
| V <sub>BG</sub>     | Buffered bandgap output <sup>3</sup>                      | 1.14                        | 1.16 | 1.18 | V    |   |

1. Maximum is highest voltage that POR is guaranteed.
2. Rising thresholds are falling threshold + hysteresis.
3. voltage Factory trimmed at V<sub>DD</sub> = 5.0 V, Temp = 125 °C


**Figure 1. Typical V<sub>DD</sub>-V<sub>OH</sub> Vs. I<sub>OH</sub> (standard drive strength) (V<sub>DD</sub> = 5 V)**

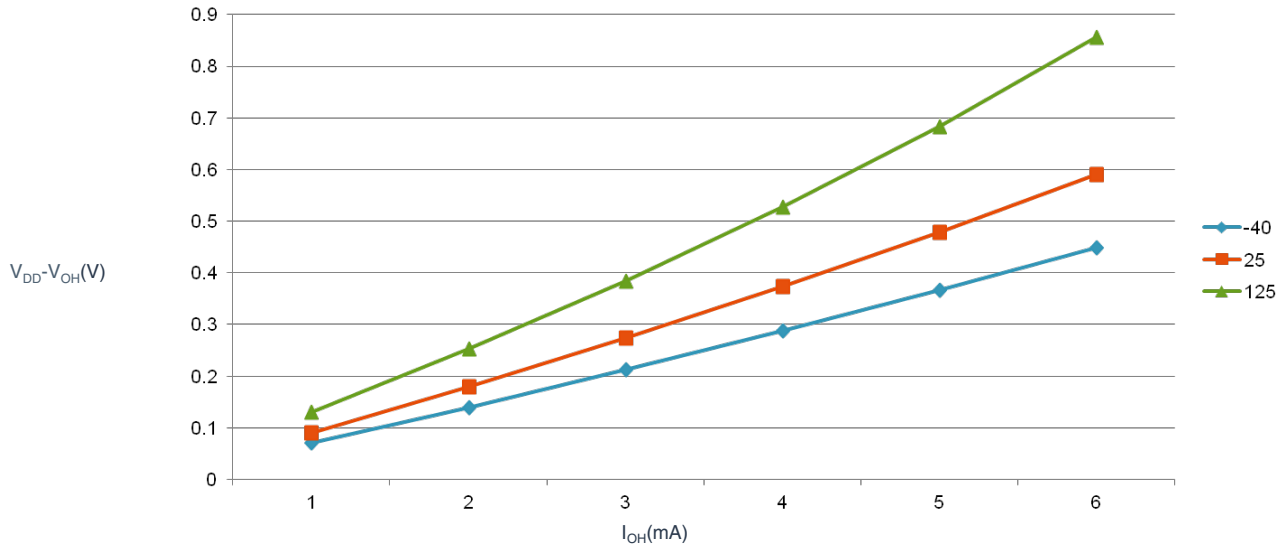


Figure 2. Typical  $V_{DD}-V_{OH}$  Vs.  $I_{OH}$  (standard drive strength) ( $V_{DD} = 3\text{ V}$ )

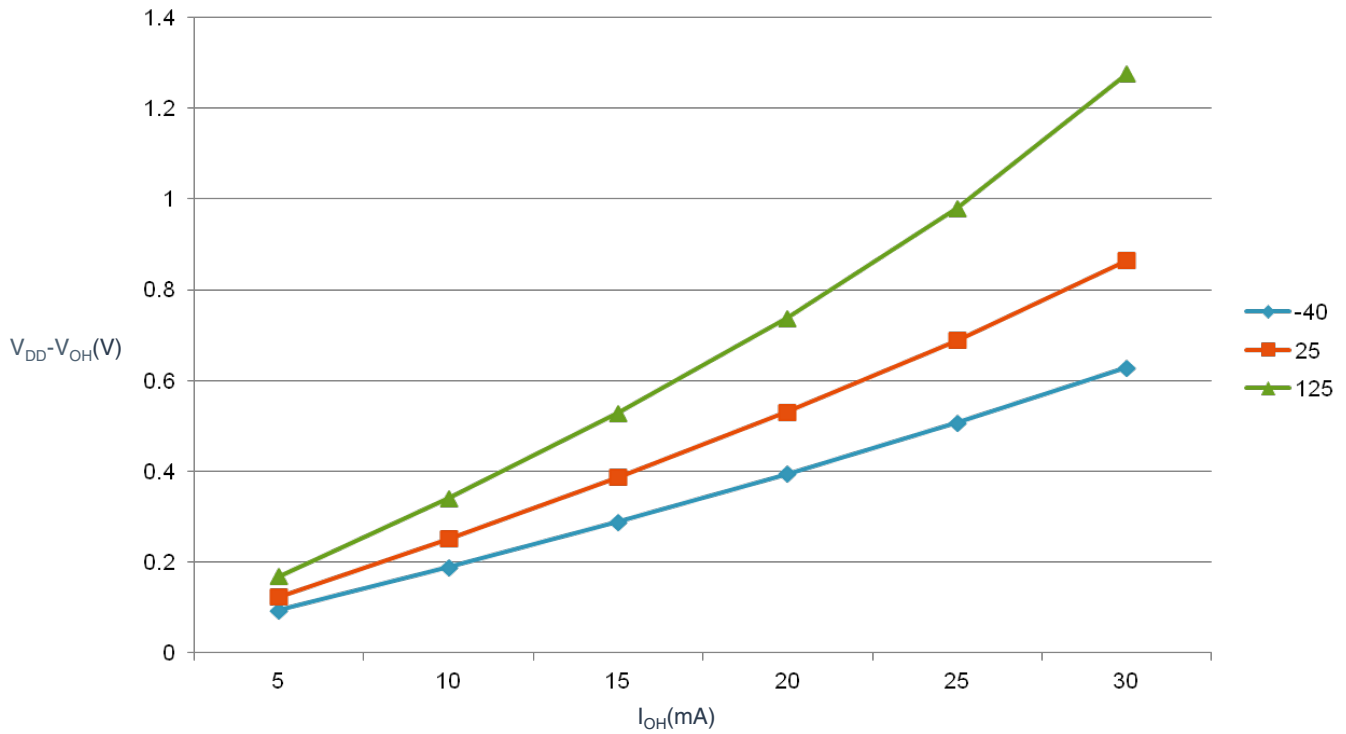


Figure 3. Typical  $V_{DD}-V_{OH}$  Vs.  $I_{OH}$  (high drive strength) ( $V_{DD} = 5\text{ V}$ )

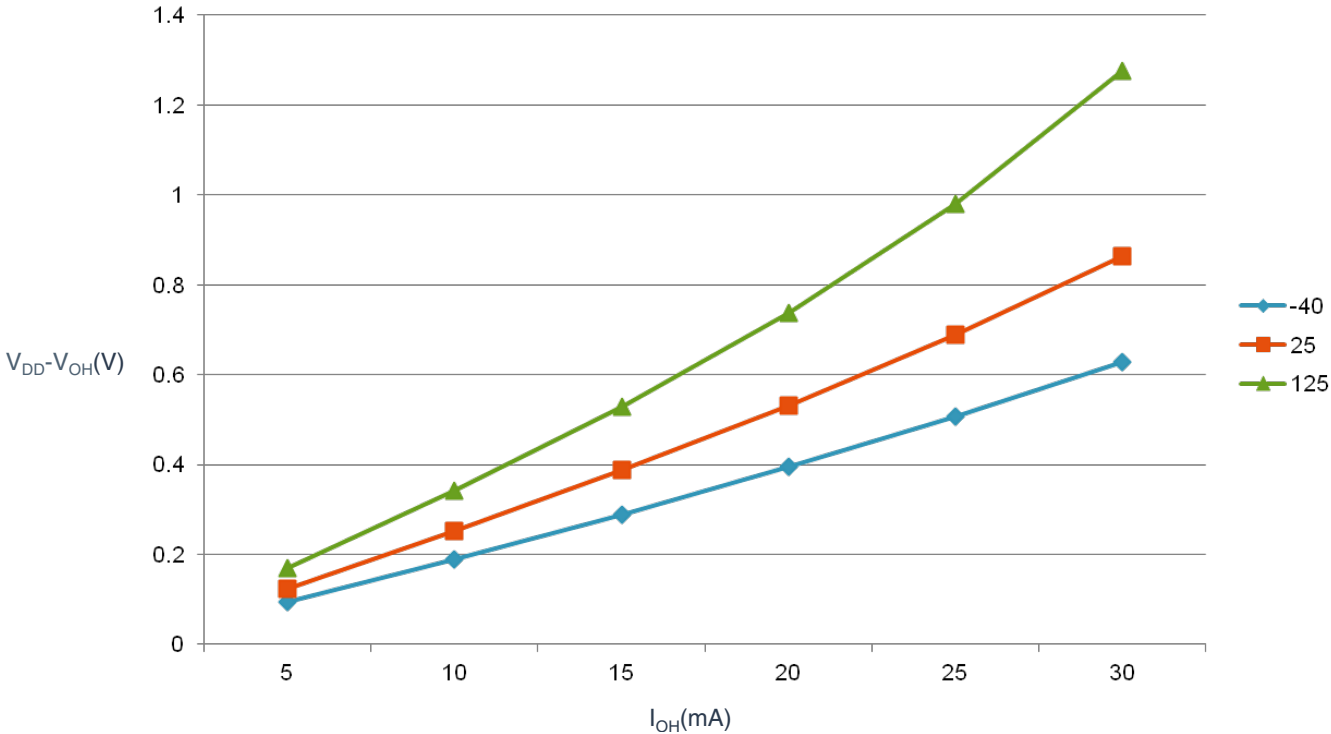


Figure 4. Typical  $V_{DD}-V_{OH}$  Vs.  $I_{OH}$  (high drive strength) ( $V_{DD} = 3\text{ V}$ )

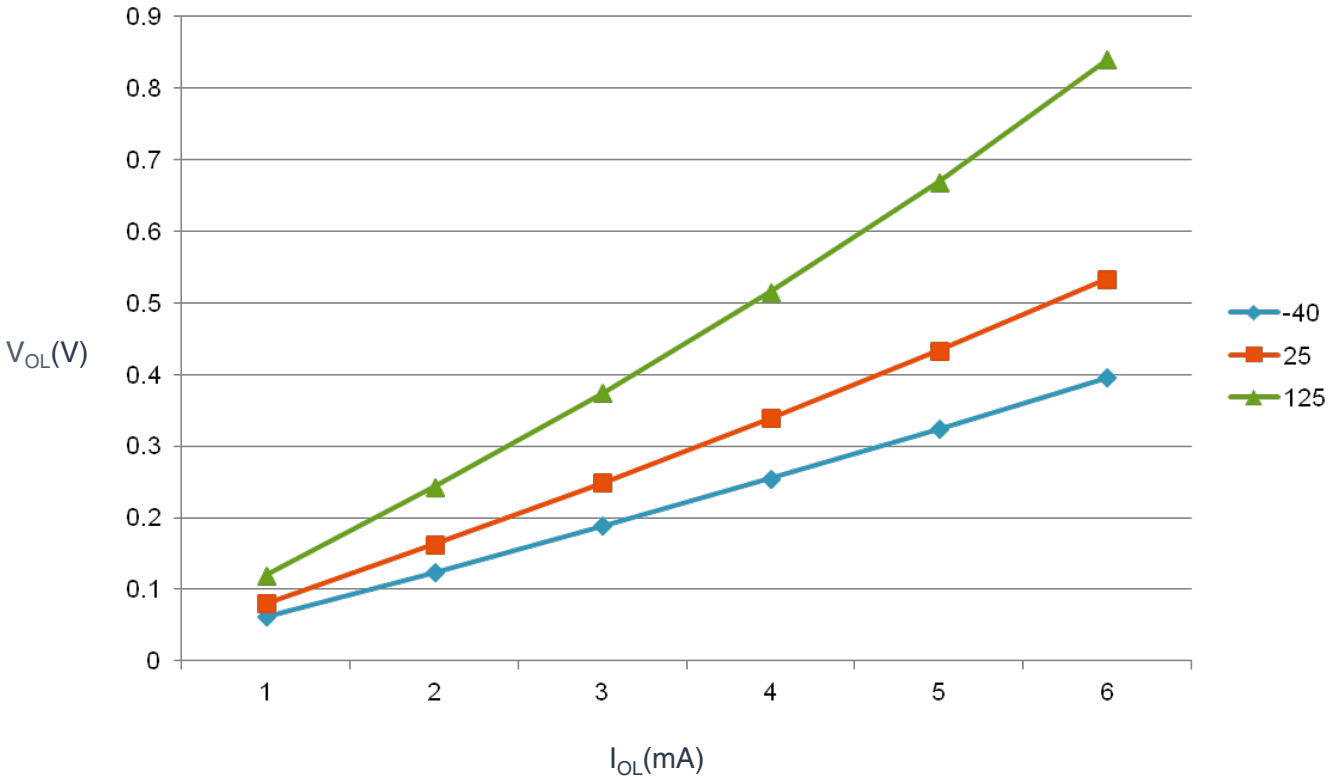


Figure 5. Typical  $V_{OL}$  Vs.  $I_{OL}$  (standard drive strength) ( $V_{DD} = 5\text{ V}$ )

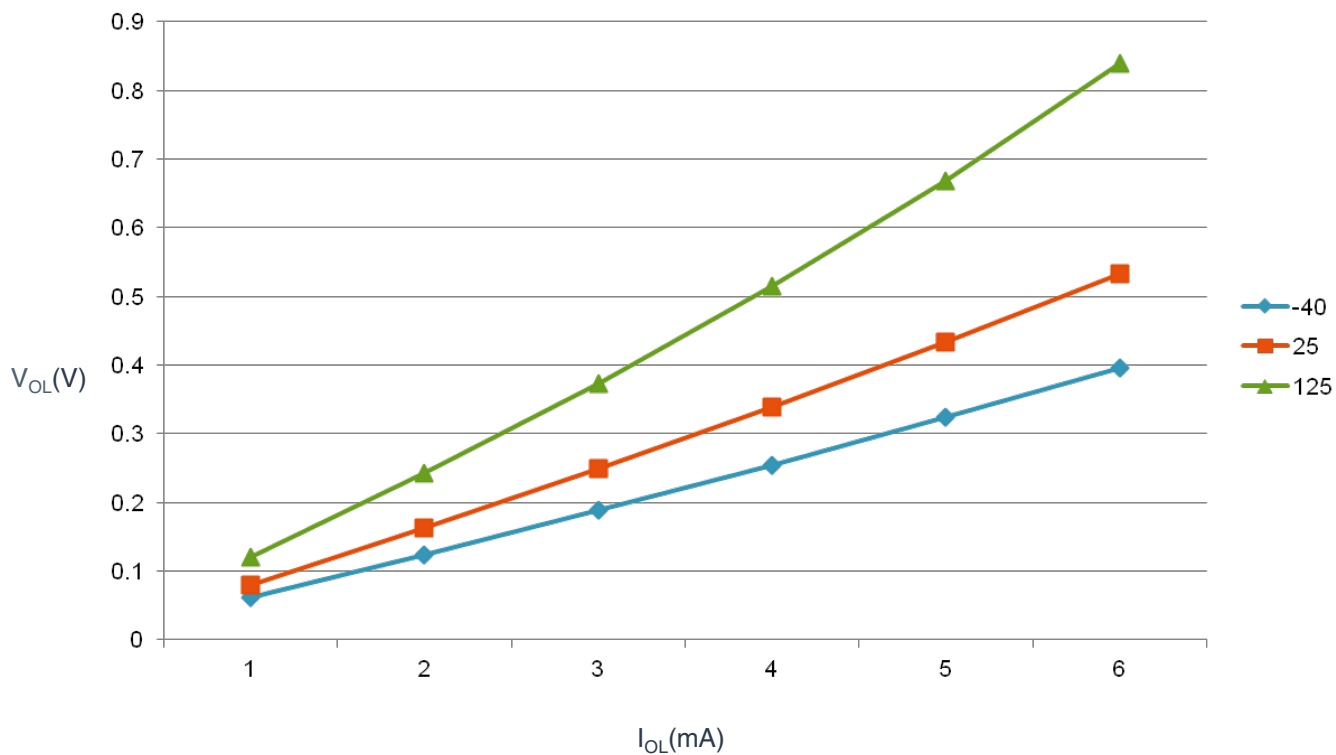


Figure 6. Typical  $V_{OL}$  Vs.  $I_{OL}$  (standard drive strength) ( $V_{DD} = 3\text{ V}$ )

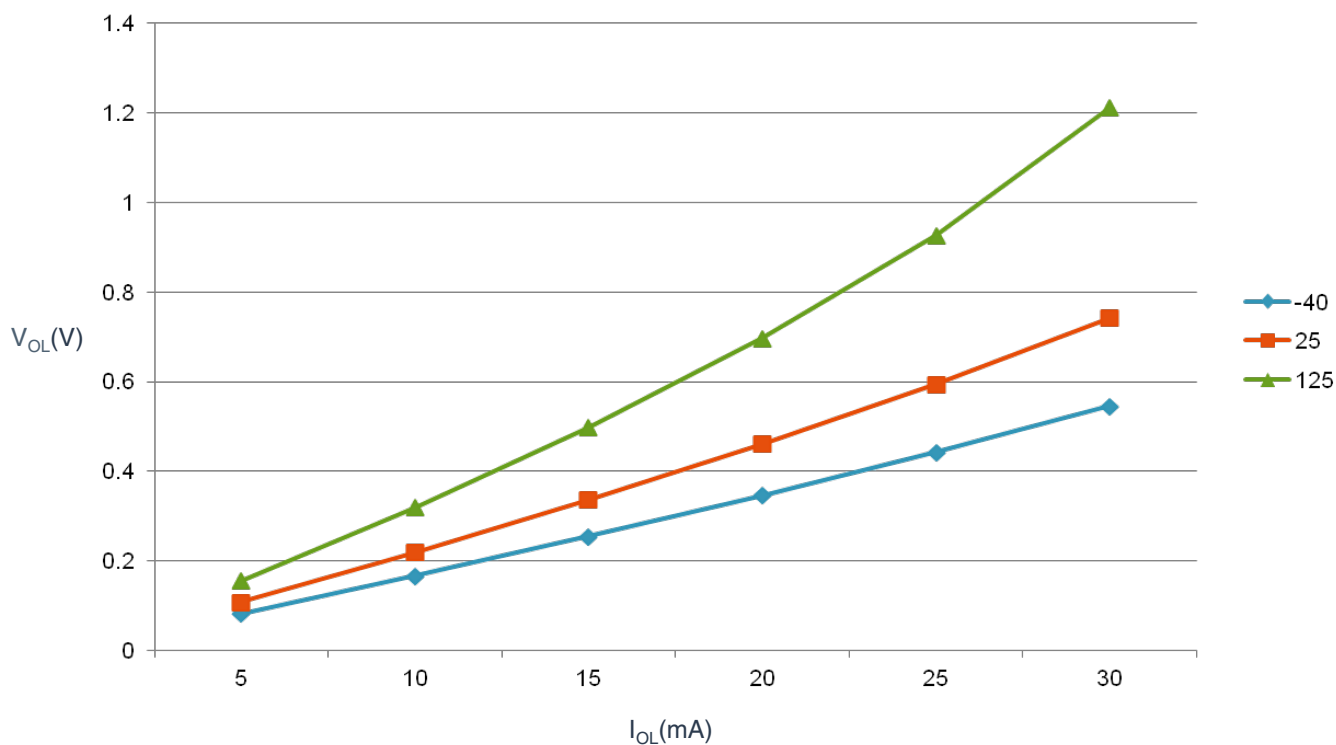


Figure 7. Typical  $V_{OL}$  Vs.  $I_{OL}$  (high drive strength) ( $V_{DD} = 5\text{ V}$ )

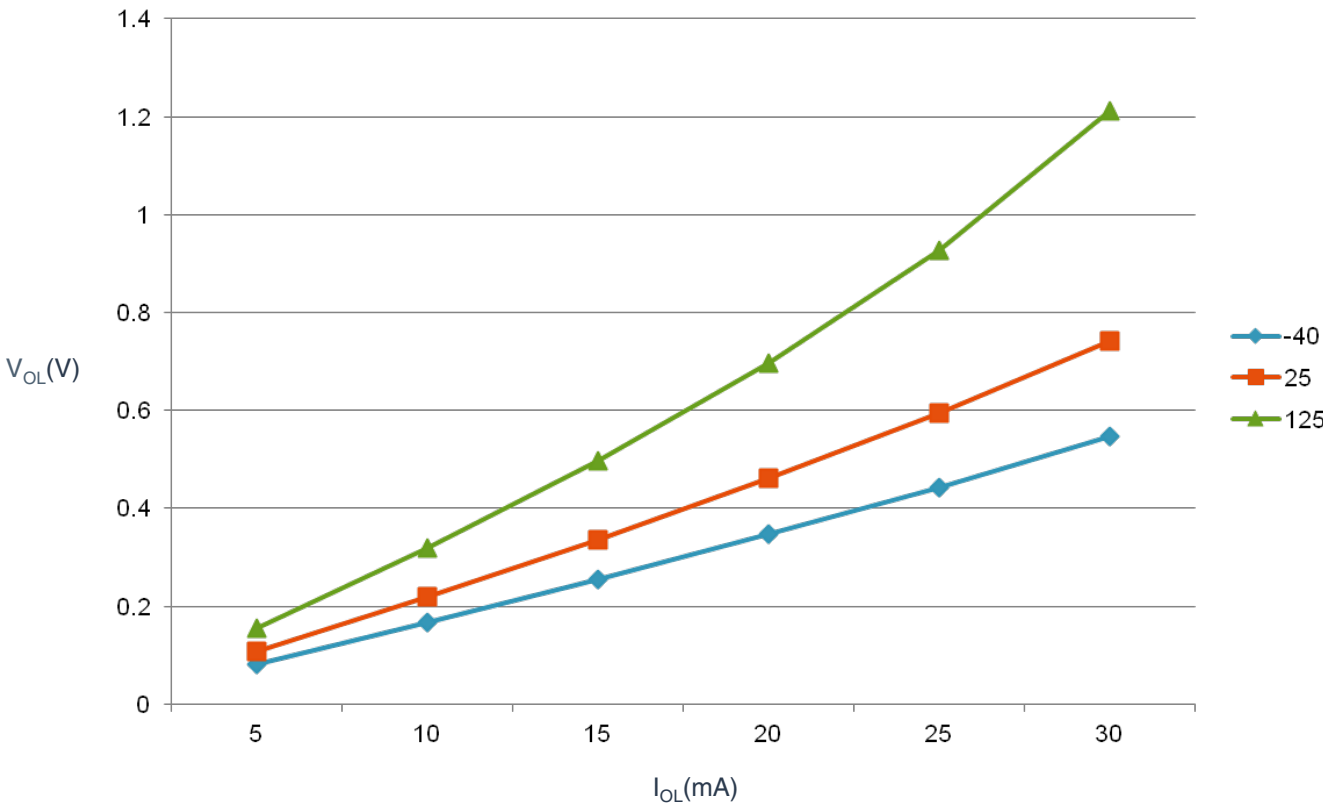


Figure 8. Typical V<sub>OL</sub> Vs. I<sub>OL</sub> (high drive strength) (V<sub>DD</sub> = 3 V)

### 4.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 4. Supply current characteristics

| Parameter  | Symbol                      | Core/Bus Freq | V <sub>DD</sub> (V) | Typical <sup>1</sup> | Max | Unit | Temp          |
|--|-----------------------------|---------------|---------------------|----------------------|-----|------|---------------|
| Run supply current FEI mode, all modules clocks enabled; run from flash            | R <sub>I<sub>DD</sub></sub> | 48/24 MHz     | 5                   | 11.1                 | —   | mA   | -40 to 125 °C |
|  |                             | 24/24 MHz     |                     | 8                    | —   |      |               |
|  |                             | 12/12 MHz     |                     | 5                    | —   |      |               |
|  |                             | 1/1 MHz       |                     | 2.4                  | —   |      |               |
|  |                             | 48/24 MHz     | 3                   | 11                   | —   |      |               |
|  |                             | 24/24 MHz     |                     | 7.9                  | —   |      |               |
|  |                             | 12/12 MHz     |                     | 4.9                  | —   |      |               |
|  |                             | 1/1 MHz       |                     | 2.3                  | —   |      |               |
| Run supply current FEI mode, all modules clocks disabled and gated; run from flash | R <sub>I<sub>DD</sub></sub> | 48/24 MHz     | 5                   | 7.8                  | —   | mA   | -40 to 125 °C |
|  |                             | 24/24 MHz     |                     | 5.5                  | —   |      |               |
|  |                             | 12/12 MHz     |                     | 3.8                  | —   |      |               |
|  |                             | 1/1 MHz       |                     | 2.3                  | —   |      |               |

Table continues on the next page...

**Table 4. Supply current characteristics (continued)**

| Parameter  | Symbol            | Core/Bus Freq | V <sub>DD</sub> (V) | Typical <sup>1</sup> | Max               | Unit | Temp          |
|--|-------------------|---------------|---------------------|----------------------|-------------------|------|---------------|
|  |                   | 48/24 MHz     | 3                   | 7.7                  | —                 |      |               |
|  |                   | 24/24 MHz     |                     | 5.4                  | —                 |      |               |
|  |                   | 12/12 MHz     |                     | 3.7                  | —                 |      |               |
|  |                   | 1/1 MHz       |                     | 2.2                  | —                 |      |               |
| Run supply current FBE mode, all modules clocks enabled; run from RAM                  | R <sub>I</sub> DD | 48/24 MHz     | 5                   | 14.7                 | —                 | mA   | -40 to 125 °C |
|  |                   | 24/24 MHz     |                     | 9.8                  | 14.9 <sup>2</sup> |      |               |
|  |                   | 12/12 MHz     |                     | 6                    | —                 |      |               |
|  |                   | 1/1 MHz       |                     | 2.4                  | —                 |      |               |
|  |                   | 48/24 MHz     | 3                   | 14.6                 | —                 |      |               |
|  |                   | 24/24 MHz     |                     | 9.6                  | 12.8 <sup>2</sup> |      |               |
|  |                   | 12/12 MHz     |                     | 5.9                  | —                 |      |               |
|  |                   | 1/1 MHz       |                     | 2.3                  | —                 |      |               |
| Run supply current FBE mode, all modules clocks disabled and gated; run from RAM       | R <sub>I</sub> DD | 48/24 MHz     | 5                   | 11.4                 | —                 | mA   | -40 to 125 °C |
|  |                   | 24/24 MHz     |                     | 7.7                  | 12.5 <sup>2</sup> |      |               |
|  |                   | 12/12 MHz     |                     | 4.7                  | —                 |      |               |
|  |                   | 1/1 MHz       |                     | 2.3                  | —                 |      |               |
|  |                   | 48/24 MHz     | 3                   | 11.3                 | —                 |      |               |
|  |                   | 24/24 MHz     |                     | 7.6                  | 9.5 <sup>2</sup>  |      |               |
|  |                   | 12/12 MHz     |                     | 4.6                  | —                 |      |               |
|  |                   | 1/1 MHz       |                     | 2.2                  | —                 |      |               |
| Wait mode current FEI mode, all modules clocks enabled                                 | W <sub>I</sub> DD | 48/24 MHz     | 5                   | 8.4                  | —                 | mA   | -40 to 125 °C |
|  |                   | 24/24 MHz     |                     | 6.5                  | 7.2 <sup>2</sup>  |      |               |
|  |                   | 12/12 MHz     |                     | 4.3                  | —                 |      |               |
|  |                   | 1/1 MHz       |                     | 2.4                  | —                 |      |               |
|  |                   | 48/24 MHz     | 3                   | 8.3                  | —                 |      |               |
|  |                   | 24/24 MHz     |                     | 6.4                  | 7.1 <sup>2</sup>  |      |               |
|  |                   | 12/12 MHz     |                     | 4.2                  | —                 |      |               |
|  |                   | 1/1 MHz       |                     | 2.3                  | —                 |      |               |
| Stop mode supply current no clocks active (except 1 kHz LPO clock) <sup>3</sup>        | S <sub>I</sub> DD | —             | 5                   | 2                    | 170 <sup>2</sup>  | μA   | -40 to 125 °C |
|  |                   | —             | 3                   | 1.9                  | 160 <sup>2</sup>  |      | -40 to 125 °C |
| ADC adder to Stop<br>ADLPC = 1<br>ADLSMP = 1<br>ADCO = 1<br>MODE = 10B<br>ADICLK = 11B | —                 | —             | 5                   | 86                   | —                 | μA   | -40 to 125 °C |
|  |                   |               | 3                   | 82                   | —                 |      |               |
| ACMP adder to Stop   | —                 | —             | 5                   | 12                   | —                 | μA   | -40 to 125 °C |
|  |                   |               | 3                   | 12                   | —                 |      |               |

Table continues on the next page...

**Table 4. Supply current characteristics (continued)**

| Parameter                      | Symbol | Core/Bus Freq | V <sub>DD</sub> (V) | Typical <sup>1</sup> | Max | Unit | Temp          |
|--------------------------------|--------|---------------|---------------------|----------------------|-----|------|---------------|
| LVD adder to Stop <sup>4</sup> | —      | —             | 5                   | 130                  | —   | μA   | -40 to 125 °C |
|                                |        |               | 3                   | 125                  | —   |      |               |

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. The high current is observed at high temperature.
3. RTC adder cause <1 μA I<sub>DD</sub> increase typically, RTC clock source is 1 kHz LPO clock.
4. LVD is periodically woken up from Stop by 5% duty cycle. The period is equal to or less than 2 ms.

### 4.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation play a significant role in EMC performance. The system designer must consult the following Freescale applications notes, available on [freescale.com](http://freescale.com) for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers
- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

## 4.2 Switching specifications

### 4.2.1 Control timing

**Table 5. Control timing**

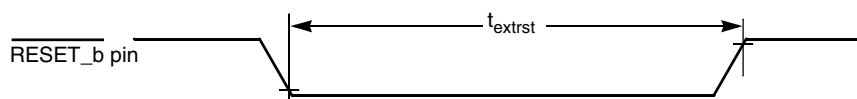
| Num | Rating   | Symbol              | Min                       | Typical <sup>1</sup> | Max  | Unit |
|-----|--|---------------------|---------------------------|----------------------|------|------|
| 1   | System and core clock                                  | f <sub>Sys</sub>    | DC                        | —                    | 48   | MHz  |
| 2   | Bus frequency (t <sub>cyc</sub> = 1/f <sub>Bus</sub> ) | f <sub>Bus</sub>    | DC                        | —                    | 24   | MHz  |
| 3   | Internal low power oscillator frequency                | f <sub>LPO</sub>    | 0.67                      | 1.0                  | 1.25 | KHz  |
| 4   | External reset pulse width <sup>2</sup>                | t <sub>extrst</sub> | 1.5 ×<br>t <sub>cyc</sub> | —                    | —    | ns   |

Table continues on the next page...

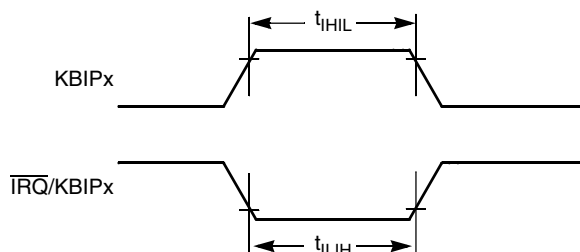
**Table 5. Control timing (continued)**

| Num | Rating  |                                | Symbol       | Min                  | Typical <sup>1</sup> | Max | Unit |
|-----|---|--------------------------------|--------------|----------------------|----------------------|-----|------|
| 5   | Reset low drive   |                                | $t_{rstdrv}$ | $34 \times t_{cyc}$  | —                    | —   | ns   |
| 6   | IRQ pulse width   | Asynchronous path <sup>2</sup> | $t_{ILIH}$   | 100                  | —                    | —   | ns   |
|     |   | Synchronous path <sup>3</sup>  | $t_{IHIL}$   | $1.5 \times t_{cyc}$ | —                    | —   | ns   |
| 7   | Keyboard interrupt pulse width  | Asynchronous path <sup>2</sup> | $t_{ILIH}$   | 100                  | —                    | —   | ns   |
|     |   | Synchronous path               | $t_{IHIL}$   | $1.5 \times t_{cyc}$ | —                    | —   | ns   |
| 8   | Port rise and fall time - Normal drive strength (load = 50 pF) <sup>4</sup> | —                              | $t_{Rise}$   | —                    | 10.2                 | —   | ns   |
|     |   | —                              | $t_{Fall}$   | —                    | 9.5                  | —   | ns   |
|     | Port rise and fall time - high drive strength (load = 50 pF) <sup>4</sup>   | —                              | $t_{Rise}$   | —                    | 5.4                  | —   | ns   |
|     |   | —                              | $t_{Fall}$   | —                    | 4.6                  | —   | ns   |

1. Typical values are based on characterization data at  $V_{DD} = 5.0\text{ V}$ ,  $25\text{ }^\circ\text{C}$  unless otherwise stated.
2. This is the shortest pulse that is guaranteed to be recognized as a RESET pin request.
3. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.
4. Timing is shown with respect to 20%  $V_{DD}$  and 80%  $V_{DD}$  levels. Temperature range  $-40\text{ }^\circ\text{C}$  to  $125\text{ }^\circ\text{C}$ .



**Figure 9. Reset timing**



**Figure 10. KBIPx timing**

### 4.2.2 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

**Table 6. FTM input timing**

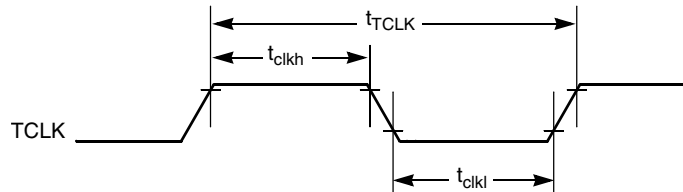
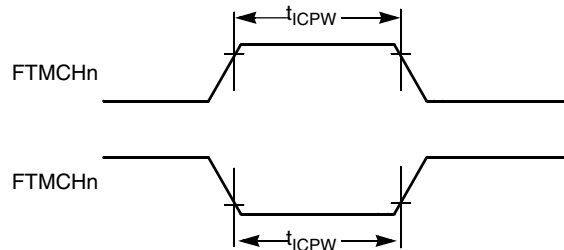
| Function                 | Symbol      | Min       | Max           | Unit |
|--------------------------|-------------|-----------|---------------|------|
| Timer clock frequency    | $f_{Timer}$ | $f_{Bus}$ | $f_{Sys}$     | Hz   |
| External clock frequency | $f_{TCLK}$  | 0         | $f_{Timer}/4$ | Hz   |

Table continues on the next page...



**Table 6. FTM input timing (continued)**

| Function                  | Symbol     | Min | Max | Unit      |
|---------------------------|------------|-----|-----|-----------|
| External clock period     | $t_{TCLK}$ | 4   | —   | $t_{cyc}$ |
| External clock high time  | $t_{clkh}$ | 1.5 | —   | $t_{cyc}$ |
| External clock low time   | $t_{clkl}$ | 1.5 | —   | $t_{cyc}$ |
| Input capture pulse width | $t_{ICPW}$ | 1.5 | —   | $t_{cyc}$ |


**Figure 11. Timer external clock**

**Figure 12. Timer input capture pulse**

## 4.3 Thermal specifications

### 4.3.1 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take  $P_{I/O}$  into account in power calculations, determine the difference between actual pin voltage and  $V_{SS}$  or  $V_{DD}$  and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and  $V_{SS}$  or  $V_{DD}$  will be very small.

**Table 7. Thermal attributes**

| Board type        | Symbol            | Description   | 64 LQFP | 80 LQFP | Unit | Notes |
|-------------------|-------------------|---|---------|---------|------|-------|
| Single-layer (1S) | R <sub>θJA</sub>  | Thermal resistance, junction to ambient (natural convection)                                    | 71      | 57      | °C/W | 1, 2  |
| Four-layer (2s2p) | R <sub>θJA</sub>  | Thermal resistance, junction to ambient (natural convection)                                    | 53      | 44      | °C/W | 1, 3  |
| Single-layer (1S) | R <sub>θJMA</sub> | Thermal resistance, junction to ambient (200 ft./min. air speed)                                | 59      | 47      | °C/W | 1, 3  |
| Four-layer (2s2p) | R <sub>θJMA</sub> | Thermal resistance, junction to ambient (200 ft./min. air speed)                                | 46      | 38      | °C/W | 1, 3  |
| —                 | R <sub>θJB</sub>  | Thermal resistance, junction to board   | 35      | 28      | °C/W | 4     |
| —                 | R <sub>θJC</sub>  | Thermal resistance, junction to case  | 20      | 15      | °C/W | 5     |
| —                 | Ψ <sub>JT</sub>   | Thermal characterization parameter, junction to package top outside center (natural convection) | 5       | 3       | °C/W | 6     |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization.

The average chip-junction temperature (T<sub>J</sub>) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Where:

T<sub>A</sub> = Ambient temperature, °C

θ<sub>JA</sub> = Package thermal resistance, junction-to-ambient, °C/W

$$P_D = P_{int} + P_{I/O}$$

P<sub>int</sub> = I<sub>DD</sub> × V<sub>DD</sub>, Watts - chip internal power

P<sub>I/O</sub> = Power dissipation on input and output pins - user determined

For most applications, P<sub>I/O</sub> << P<sub>int</sub> and can be neglected. An approximate relationship between P<sub>D</sub> and T<sub>J</sub> (if P<sub>I/O</sub> is neglected) is:

$$P_D = K \div (T_J + 273 \text{ } ^\circ\text{C})$$

Solving the equations above for K gives:

$$K = P_D \times (T_A + 273 \text{ } ^\circ\text{C}) + \theta_{JA} \times (P_D)^2$$

where  $K$  is a constant pertaining to the particular part.  $K$  can be determined by measuring  $P_D$  (at equilibrium) for an known  $T_A$ . Using this value of  $K$ , the values of  $P_D$  and  $T_J$  can be obtained by solving the above equations iteratively for any value of  $T_A$ .

## 5 Peripheral operating requirements and behaviors

### 5.1 Core modules

#### 5.1.1 SWD electricals

Table 8. SWD full voltage range electricals

| Symbol | Description  | Min. | Max. | Unit |
|--------|--|------|------|------|
|        | Operating voltage  | 2.7  | 5.5  | V    |
| J1     | SWD_CLK frequency of operation <ul style="list-style-type: none"> <li>Serial wire debug</li> </ul> | 0    | 24   | MHz  |
| J2     | SWD_CLK cycle period   | 1/J1 | —    | ns   |
| J3     | SWD_CLK clock pulse width <ul style="list-style-type: none"> <li>Serial wire debug</li> </ul>      | 20   | —    | ns   |
| J4     | SWD_CLK rise and fall times  | —    | 3    | ns   |
| J9     | SWD_DIO input data setup time to SWD_CLK rise  | 10   | —    | ns   |
| J10    | SWD_DIO input data hold time after SWD_CLK rise  | 3    | —    | ns   |
| J11    | SWD_CLK high to SWD_DIO data valid   | —    | 35   | ns   |
| J12    | SWD_CLK high to SWD_DIO high-Z   | 5    | —    | ns   |

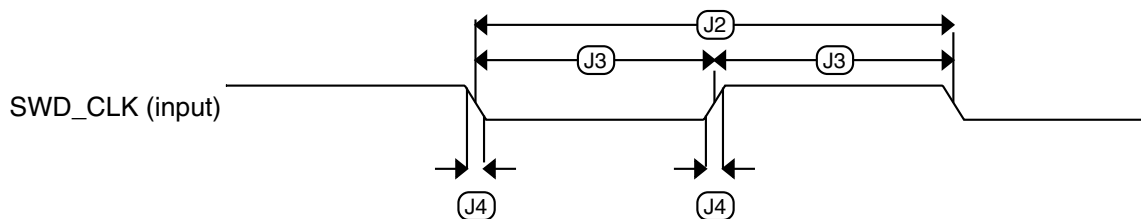


Figure 13. Serial wire clock input timing

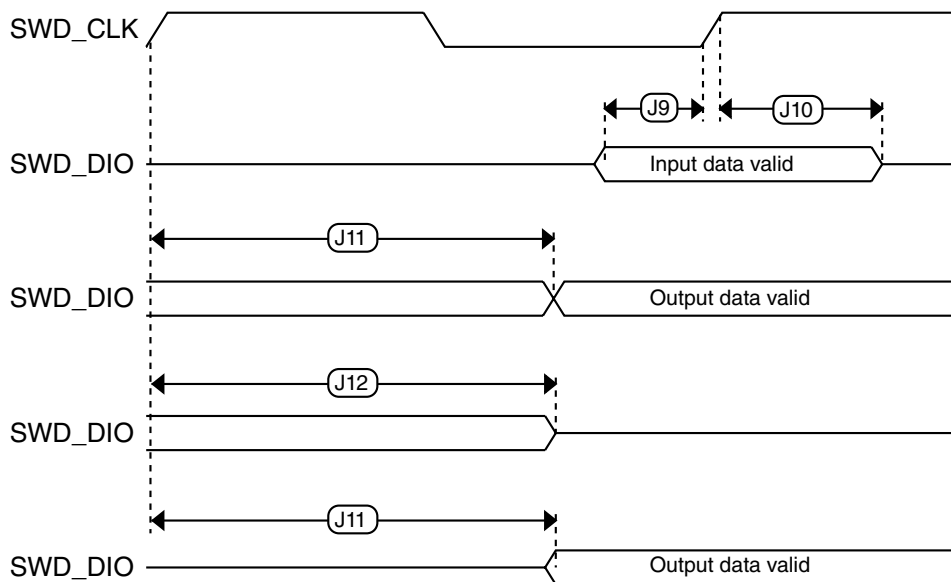


Figure 14. Serial wire data timing

## 5.2 External oscillator (OSC) and ICS characteristics

Table 9. OSC and ICS specifications (temperature range = -40 to 125 °C ambient)

| Num | Characteristic                                   |  | Symbol   | Min                   | Typical <sup>1</sup> | Max     | Unit |
|-----|--|--|----------|-----------------------|----------------------|---------|------|
| 1   | Crystal or resonator frequency                   | Low range (RANGE = 0)                      | $f_{lo}$ | 31.25                 | 32.768               | 39.0625 | kHz  |
|     |  | High range (RANGE = 1)                     | $f_{hi}$ | 4                     | —                    | 24      | MHz  |
| 2   | Load capacitors                                  |  | C1, C2   | See Note <sup>2</sup> |                      |         |      |
| 3   | Feedback resistor                                | Low Frequency, Low-Power Mode <sup>3</sup> | $R_F$    | —                     | —                    | —       | MΩ   |
|     |  | Low Frequency, High-Gain Mode              |          | —                     | 10                   | —       | MΩ   |
|     |  | High Frequency, Low-Power Mode             |          | —                     | 1                    | —       | MΩ   |
|     |  | High Frequency, High-Gain Mode             |          | —                     | 1                    | —       | MΩ   |
| 4   | Series resistor - Low Frequency                  | Low-Power Mode <sup>3</sup>                | $R_S$    | —                     | 0                    | —       | kΩ   |
|     |  | High-Gain Mode                             |          | —                     | 200                  | —       | kΩ   |
| 5   | Series resistor - High Frequency                 | Low-Power Mode <sup>3</sup>                | $R_S$    | —                     | 0                    | —       | kΩ   |
|     | Series resistor - High Frequency, High-Gain Mode | 4 MHz                                      |          | —                     | 0                    | —       | kΩ   |
|     |  | 8 MHz                                      |          | —                     | 0                    | —       | kΩ   |

Table continues on the next page...

**Table 9. OSC and ICS specifications (temperature range = -40 to 125 °C ambient) (continued)**

| Num | Characteristic   |  | Symbol               | Min   | Typical <sup>1</sup> | Max     | Unit        |
|-----|--|--|----------------------|-------|----------------------|---------|-------------|
|     |  | 16 MHz   |                      | —     | 0                    | —       | kΩ          |
| 6   | Crystal start-up time low range = 32.768 kHz crystal; High range = 20 MHz crystal <sup>4,5</sup> | Low range, low power                                       | $t_{CSTL}$           | —     | 1000                 | —       | ms          |
|     |  | Low range, high gain                                       |                      | —     | 800                  | —       | ms          |
|     |  | High range, low power                                      | $t_{CSTH}$           | —     | 3                    | —       | ms          |
|     |  | High range, high gain                                      |                      | —     | 1.5                  | —       | ms          |
| 7   | Internal reference start-up time   |  | $t_{IRST}$           | —     | 20                   | 50      | μs          |
| 8   | Internal reference clock (IRC) frequency trim range  |  | $f_{int\_t}$         | 31.25 | —                    | 39.0625 | kHz         |
| 9   | Internal reference clock frequency, factory trimmed  | T = 125 °C, V <sub>DD</sub> = 5 V                          | $f_{int\_ft}$        | —     | 37.5                 | —       | kHz         |
| 10  | DCO output frequency range   | FLL reference = $f_{int\_t}$ , $f_{lo}$ , or $f_{hi}/RDIV$ | $f_{dco}$            | 40    | —                    | 50      | MHz         |
| 11  | Factory trimmed internal oscillator accuracy   | T = 125 °C, V <sub>DD</sub> = 5 V                          | $\Delta f_{int\_ft}$ | -0.8  | —                    | 0.8     | %           |
| 12  | Deviation of IRC over temperature when trimmed at T = 25 °C, V <sub>DD</sub> = 5 V               | Over temperature range from -40 °C to 125 °C               | $\Delta f_{int\_t}$  | -1    | —                    | 0.8     | %           |
| 13  | Frequency accuracy of DCO output using factory trim value  | Over temperature range from -40 °C to 125 °C               | $\Delta f_{dco\_ft}$ | -2.3  | —                    | 0.8     | %           |
| 14  | FLL acquisition time <sup>4,6</sup>  |  | $t_{Acquire}$        | —     | —                    | 2       | ms          |
| 15  | Long term jitter of DCO output clock (averaged over 2 ms interval) <sup>7</sup>                  |  | $C_{Jitter}$         | —     | 0.02                 | 0.2     | % $f_{dco}$ |

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. See crystal or resonator manufacturer's recommendation.
3. Load capacitors (C<sub>1</sub>, C<sub>2</sub>), feedback resistor (R<sub>F</sub>) and series resistor (R<sub>S</sub>) are incorporated internally when RANGE = HGO = 0.
4. This parameter is characterized and not tested on each device.
5. Proper PC board layout procedures must be followed to achieve specifications.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f<sub>Bus</sub>. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V<sub>DD</sub> and V<sub>SS</sub> and variation in crystal oscillator frequency increase the C<sub>Jitter</sub> percentage for a given interval.

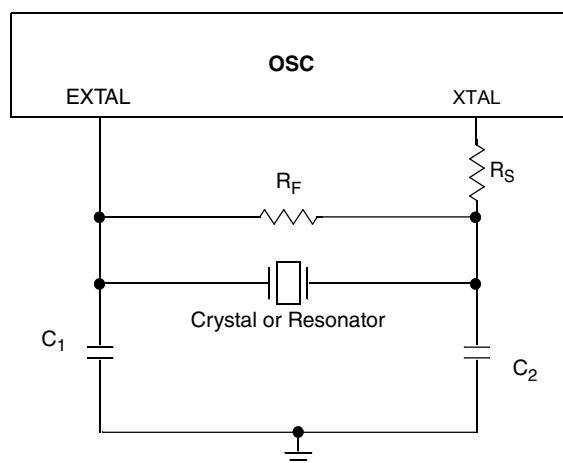


Figure 15. Typical crystal or resonator circuit

### 5.3 NVM specifications

This section provides details about program/erase times and program/erase endurance for the flash memories.

Table 10. Flash characteristics

| Characteristic   | Symbol           | Min <sup>1</sup> | Typical <sup>2</sup> | Max <sup>3</sup> | Unit <sup>4</sup> |
|--|------------------|------------------|----------------------|------------------|-------------------|
| Supply voltage for program/erase -40 °C to 125 °C                  | $V_{prog/erase}$ | 2.7              | —                    | 5.5              | V                 |
| Supply voltage for read operation                                  | $V_{Read}$       | 2.7              | —                    | 5.5              | V                 |
| NVM Bus frequency  | $f_{NVMBUS}$     | 1                | —                    | 24               | MHz               |
| NVM Operating frequency  | $f_{NVMOP}$      | 0.8              | 1                    | 1.05             | MHz               |
| Erase Verify All Blocks  | $t_{VFYALL}$     | —                | —                    | 2605             | $t_{cyc}$         |
| Erase Verify Flash Block   | $t_{RD1BLK}$     | —                | —                    | 2579             | $t_{cyc}$         |
| Erase Verify Flash Section   | $t_{RD1SEC}$     | —                | —                    | 485              | $t_{cyc}$         |
| Read Once  | $t_{RDONCE}$     | —                | —                    | 464              | $t_{cyc}$         |
| Program Flash (2 word)   | $t_{PGM2}$       | 0.12             | 0.13                 | 0.31             | ms                |
| Program Flash (4 word)   | $t_{PGM4}$       | 0.21             | 0.21                 | 0.49             | ms                |
| Program Once   | $t_{PGMONCE}$    | 0.20             | 0.21                 | 0.21             | ms                |
| Erase All Blocks   | $t_{ERSALL}$     | 95.42            | 100.18               | 100.30           | ms                |
| Erase Flash Block  | $t_{ERSBLK}$     | 95.42            | 100.18               | 100.30           | ms                |
| Erase Flash Sector   | $t_{ERSPG}$      | 19.10            | 20.05                | 20.09            | ms                |
| Unsecure Flash   | $t_{UNSECU}$     | 95.42            | 100.19               | 100.31           | ms                |
| Verify Backdoor Access Key   | $t_{VFYKEY}$     | —                | —                    | 482              | $t_{cyc}$         |
| Set User Margin Level  | $t_{MLOADU}$     | —                | —                    | 415              | $t_{cyc}$         |
| FLASH Program/erase endurance $T_L$ to $T_H$<br>= -40 °C to 125 °C | $\eta_{FLPE}$    | 10 k             | 100 k                | —                | Cycles            |

Table continues on the next page...

**Table 10. Flash characteristics (continued)**

| Characteristic   | Symbol       | Min <sup>1</sup> | Typical <sup>2</sup> | Max <sup>3</sup> | Unit <sup>4</sup> |
|--|--------------|------------------|----------------------|------------------|-------------------|
| Data retention at an average junction temperature of $T_{Javg} = 85^{\circ}\text{C}$ after up to 10,000 program/erase cycles | $t_{D\_ret}$ | 15               | 100                  | —                | years             |

1. Minimum times are based on maximum  $f_{NVMOP}$  and maximum  $f_{NVMBUS}$
2. Typical times are based on typical  $f_{NVMOP}$  and maximum  $f_{NVMBUS}$
3. Maximum times are based on typical  $f_{NVMOP}$  and typical  $f_{NVMBUS}$  plus aging
4.  $t_{cyc} = 1 / f_{NVMBUS}$

Program and erase operations do not require any special power sources other than the normal  $V_{DD}$  supply. For more detailed information about program/erase operations, see the Flash Memory Module section in the reference manual.

## 5.4 Analog

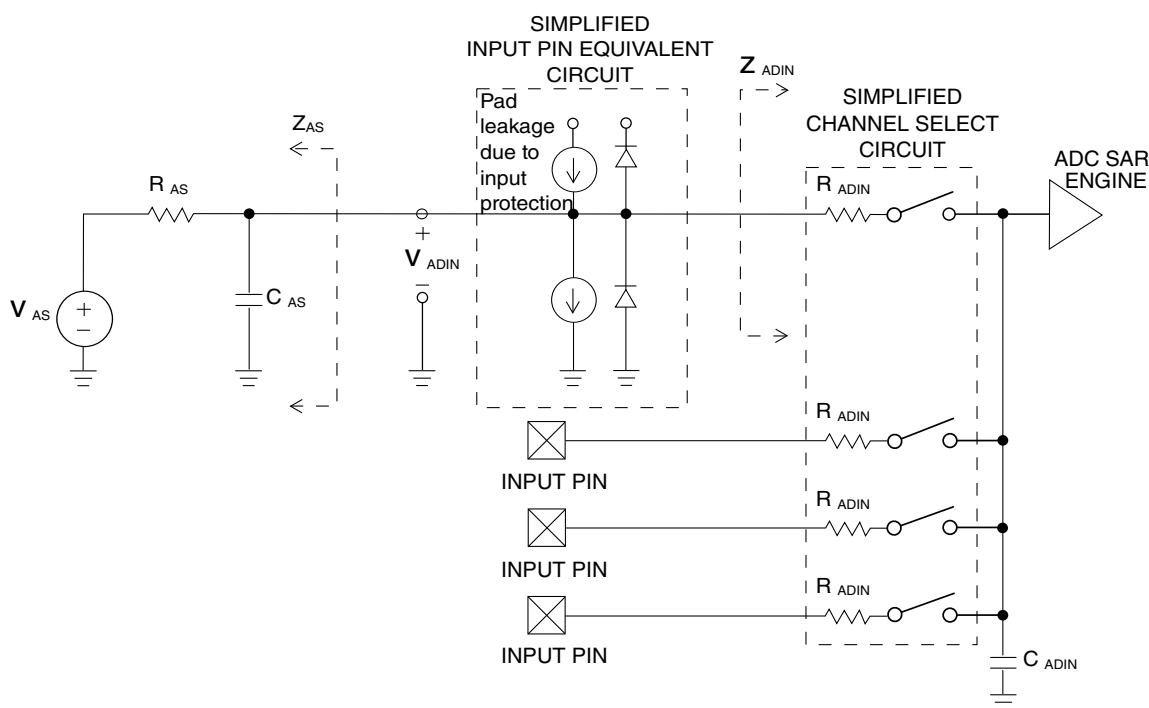
### 5.4.1 ADC characteristics

**Table 11. 5 V 12-bit ADC operating conditions**

| Characteristic                        | Conditions                               | Symbol           | Min         | Typ <sup>1</sup> | Max         | Unit       | Comment         |
|---------------------------------------|--|------------------|-------------|------------------|-------------|------------|-----------------|
| Reference potential                   | • Low                                    | $V_{REFL}$       | $V_{SSA}$   | —                | $V_{DDA}/2$ | V          | —               |
|                                       | • High                                   | $V_{REFH}$       | $V_{DDA}/2$ | —                | $V_{DDA}$   |            |                 |
| Supply voltage                        | Absolute                                 | $V_{DDA}$        | 2.7         | —                | 5.5         | V          | —               |
|                                       | Delta to $V_{DD}$ ( $V_{DD} - V_{DDA}$ ) | $\Delta V_{DDA}$ | -100        | 0                | +100        | mV         | —               |
| Input voltage                         |  | $V_{ADIN}$       | $V_{REFL}$  | —                | $V_{REFH}$  | V          | —               |
| Input capacitance                     |  | $C_{ADIN}$       | —           | 4.5              | 5.5         | pF         | —               |
| Input resistance                      |  | $R_{ADIN}$       | —           | 3                | 5           | k $\Omega$ | —               |
| Analog source resistance              | 12-bit mode                              | $R_{AS}$         | —           | —                | 2           | k $\Omega$ | External to MCU |
|                                       | • $f_{ADCK} > 4$ MHz                     |                  | —           | —                | 5           |            |                 |
|                                       | • $f_{ADCK} < 4$ MHz                     |                  | —           | —                | 5           |            |                 |
| 10-bit mode                           | —  | —                | 5           | 10               |             |            |                 |
| • $f_{ADCK} > 4$ MHz                  | —  | —                | 10          |                  |             |            |                 |
| • $f_{ADCK} < 4$ MHz                  | —  | —                | 10          |                  |             |            |                 |
| 8-bit mode<br>(all valid $f_{ADCK}$ ) | —  | —                | 10          |                  |             |            |                 |
| ADC conversion clock frequency        | High speed (ADLPC=0)                     | $f_{ADCK}$       | 0.4         | —                | 8.0         | MHz        | —               |
|                                       | Low power (ADLPC=1)                      |                  | 0.4         | —                | 4.0         |            |                 |

## Peripheral operating requirements and behaviors

1. Typical values assume  $V_{DDA} = 5.0\text{ V}$ ,  $\text{Temp} = 25^\circ\text{C}$ ,  $f_{\text{ADCK}} = 1.0\text{ MHz}$  unless otherwise stated. Typical values are for reference only and are not tested in production.



**Figure 16. ADC input impedance equivalency diagram**

**Table 12. 12-bit ADC characteristics ( $V_{\text{REFH}} = V_{\text{DDA}}$ ,  $V_{\text{REFL}} = V_{\text{SSA}}$ )**

| Characteristic  | Conditions              | Symbol           | Min | Typ <sup>1</sup> | Max | Unit          |
|---|-------------------------|------------------|-----|------------------|-----|---------------|
| Supply current<br>ADLPC = 1<br>ADLSMP = 1<br>ADCO = 1 |                         | $I_{\text{DDA}}$ | —   | 133              | —   | $\mu\text{A}$ |
| Supply current<br>ADLPC = 1<br>ADLSMP = 0<br>ADCO = 1 |                         | $I_{\text{DDA}}$ | —   | 218              | —   | $\mu\text{A}$ |
| Supply current<br>ADLPC = 0<br>ADLSMP = 1<br>ADCO = 1 |                         | $I_{\text{DDA}}$ | —   | 327              | —   | $\mu\text{A}$ |
| Supply current<br>ADLPC = 0<br>ADLSMP = 0<br>ADCO = 1 |                         | $I_{\text{DDA}}$ | —   | 582              | 990 | $\mu\text{A}$ |
| Supply current  | Stop, reset, module off | $I_{\text{DDA}}$ | —   | 0.011            | 1   | $\mu\text{A}$ |

Table continues on the next page...



**Table 12. 12-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

| Characteristic                          | Conditions                | Symbol       | Min                    | Typ <sup>1</sup> | Max  | Unit             |
|---|---------------------------|--------------|------------------------|------------------|------|------------------|
| ADC asynchronous clock source           | High speed (ADLPC = 0)    | $f_{ADACK}$  | 2                      | 3.3              | 5    | MHz              |
|   | Low power (ADLPC = 1)     |              | 1.25                   | 2                | 3.3  |                  |
| Conversion time (including sample time) | Short sample (ADLSMP = 0) | $t_{ADC}$    | —                      | 20               | —    | ADCK cycles      |
|   | Long sample (ADLSMP = 1)  |              | —                      | 40               | —    |                  |
| Sample time                             | Short sample (ADLSMP = 0) | $t_{ADS}$    | —                      | 3.5              | —    | ADCK cycles      |
|   | Long sample (ADLSMP = 1)  |              | —                      | 23.5             | —    |                  |
| Total unadjusted Error <sup>2</sup>     | 12-bit mode               | $E_{TUE}$    | —                      | ±5.0             | —    | LSB <sup>3</sup> |
|   | 10-bit mode               |              | —                      | ±1.5             | —    |                  |
|   | 8-bit mode                |              | —                      | ±0.8             | —    |                  |
| Differential Non-Linearity              | 12-bit mode               | DNL          | —                      | ±1.5             | —    | LSB <sup>3</sup> |
|   | 10-bit mode               |              | —                      | ±0.4             | —    |                  |
|   | 8-bit mode                |              | —                      | ±0.15            | —    |                  |
| Integral Non-Linearity                  | 12-bit mode               | INL          | —                      | ±1.5             | —    | LSB <sup>3</sup> |
|   | 10-bit mode               |              | —                      | ±0.4             | —    |                  |
|   | 8-bit mode                |              | —                      | ±0.15            | —    |                  |
| Zero-scale error <sup>4</sup>           | 12-bit mode               | $E_{ZS}$     | —                      | ±1.0             | —    | LSB <sup>3</sup> |
|   | 10-bit mode               |              | —                      | ±0.2             | —    |                  |
|   | 8-bit mode                |              | —                      | ±0.35            | —    |                  |
| Full-scale error <sup>5</sup>           | 12-bit mode               | $E_{FS}$     | —                      | ±2.5             | —    | LSB <sup>3</sup> |
|   | 10-bit mode               |              | —                      | ±0.3             | —    |                  |
|   | 8-bit mode                |              | —                      | ±0.25            | —    |                  |
| Quantization error                      | ≤12 bit modes             | $E_Q$        | —                      | —                | ±0.5 | LSB <sup>3</sup> |
| Input leakage error <sup>6</sup>        | all modes                 | $E_{IL}$     | $I_{in} \times R_{AS}$ |                  |      | mV               |
| Temp sensor slope                       | -40 °C–25 °C              | m            | —                      | 3.266            | —    | mV/°C            |
|   | 25 °C–125 °C              |              | —                      | 3.638            | —    |                  |
| Temp sensor voltage                     | 25 °C                     | $V_{TEMP25}$ | —                      | 1.396            | —    | V                |

1. Typical values assume  $V_{DDA} = 5.0$  V, Temp = 25 °C,  $f_{ADCK} = 1.0$  MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Includes quantization
3.  $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
4.  $V_{ADIN} = V_{SSA}$
5.  $V_{ADIN} = V_{DDA}$
6.  $I_{in}$  = leakage current (refer to DC characteristics)

## 5.4.2 Analog comparator (ACMP) electricals

**Table 13. Comparator electrical specifications**

| Characteristic                        | Symbol       | Min            | Typical | Max       | Unit    |
|---------------------------------------|--------------|----------------|---------|-----------|---------|
| Supply voltage                        | $V_{DDA}$    | 2.7            | —       | 5.5       | V       |
| Supply current (Operation mode)       | $I_{DDA}$    | —              | 10      | 20        | $\mu$ A |
| Analog input voltage                  | $V_{AIN}$    | $V_{SS} - 0.3$ | —       | $V_{DDA}$ | V       |
| Analog input offset voltage           | $V_{AIO}$    | —              | —       | 40        | mV      |
| Analog comparator hysteresis (HYST=0) | $V_H$        | —              | 15      | 20        | mV      |
| Analog comparator hysteresis (HYST=1) | $V_H$        | —              | 20      | 30        | mV      |
| Supply current (Off mode)             | $I_{DDAOFF}$ | —              | 60      | —         | nA      |
| Propagation Delay                     | $t_D$        | —              | 0.4     | 1         | $\mu$ s |

## 5.5 Communication interfaces

### 5.5.1 SPI switching specifications

The serial peripheral interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's reference manual for information about the modified transfer formats used for communicating with slower peripheral devices. All timing is shown with respect to 20%  $V_{DD}$  and 80%  $V_{DD}$ , unless noted, and 25 pF load on all SPI pins. All timing assumes slew rate control is disabled and high-drive strength is enabled for SPI output pins.

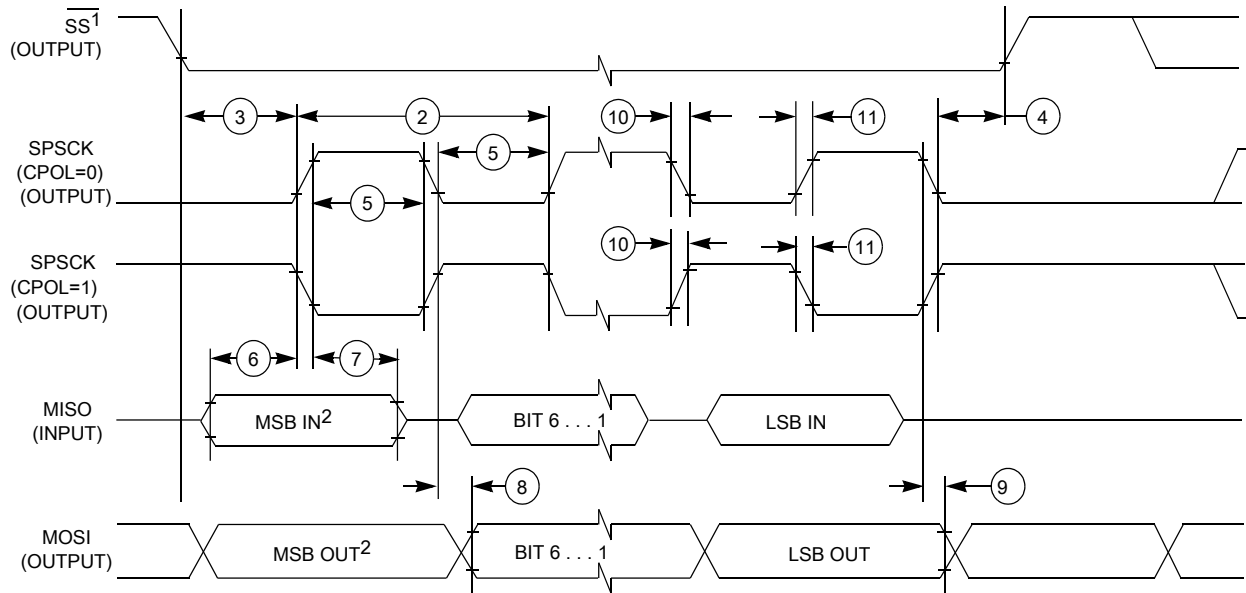
**Table 14. SPI master mode timing**

| Num. | Symbol       | Description                    | Min.               | Max.                  | Unit        | Comment                    |
|------|--------------|--------------------------------|--------------------|-----------------------|-------------|----------------------------|
| 1    | $f_{op}$     | Frequency of operation         | $f_{Bus}/2048$     | $f_{Bus}/2$           | Hz          | $f_{Bus}$ is the bus clock |
| 2    | $t_{SPSCK}$  | SPSCK period                   | $2 \times t_{Bus}$ | $2048 \times t_{Bus}$ | ns          | $t_{Bus} = 1/f_{Bus}$      |
| 3    | $t_{Lead}$   | Enable lead time               | 1/2                | —                     | $t_{SPSCK}$ | —                          |
| 4    | $t_{Lag}$    | Enable lag time                | 1/2                | —                     | $t_{SPSCK}$ | —                          |
| 5    | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{Bus} - 30$     | $1024 \times t_{Bus}$ | ns          | —                          |
| 6    | $t_{SU}$     | Data setup time (inputs)       | 8                  | —                     | ns          | —                          |
| 7    | $t_{HI}$     | Data hold time (inputs)        | 8                  | —                     | ns          | —                          |
| 8    | $t_v$        | Data valid (after SPSCK edge)  | —                  | 25                    | ns          | —                          |
| 9    | $t_{HO}$     | Data hold time (outputs)       | 20                 | —                     | ns          | —                          |

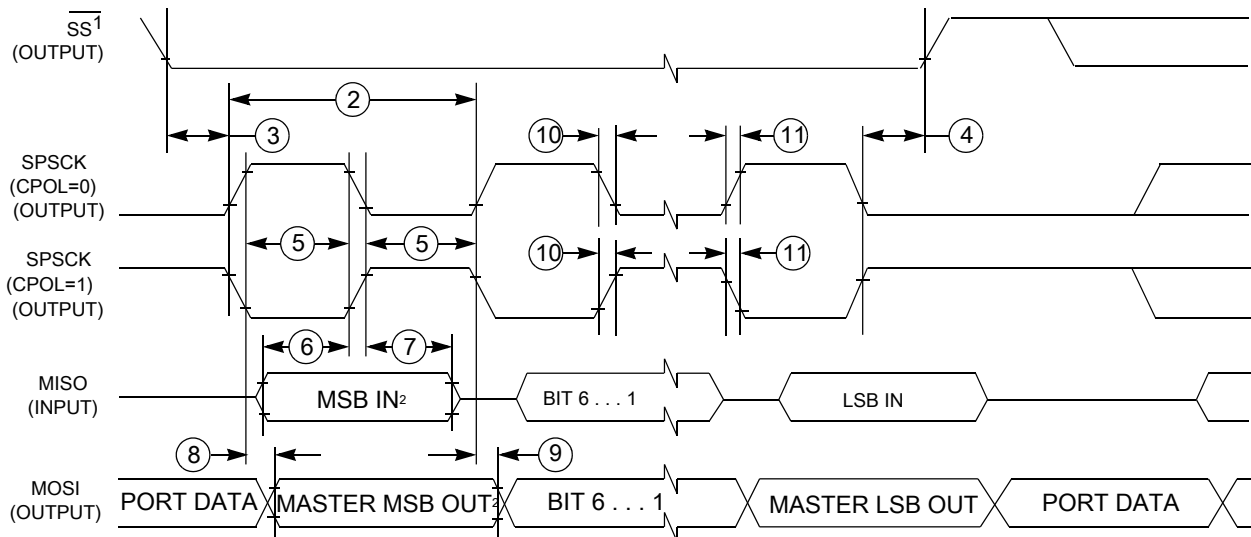
Table continues on the next page...

**Table 14. SPI master mode timing (continued)**

| Nu m. | Symbol   | Description      | Min. | Max.           | Unit | Comment |
|-------|----------|------------------|------|----------------|------|---------|
| 10    | $t_{RI}$ | Rise time input  | —    | $t_{Bus} - 25$ | ns   | —       |
|       | $t_{FI}$ | Fall time input  |      |                |      |         |
| 11    | $t_{RO}$ | Rise time output | —    | 25             | ns   | —       |
|       | $t_{FO}$ | Fall time output |      |                |      |         |



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

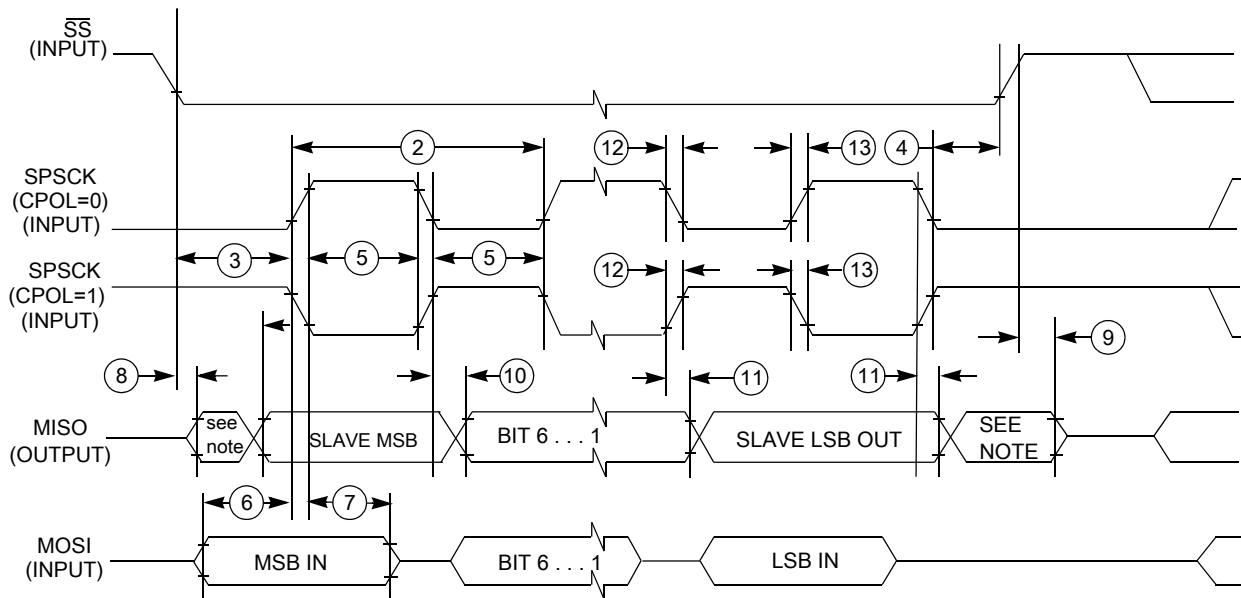
**Figure 17. SPI master mode timing (CPHA=0)**


1. If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 18. SPI master mode timing (CPHA=1)**

**Table 15. SPI slave mode timing**

| Nu m. | Symbol       | Description                    | Min.               | Max.           | Unit      | Comment   |
|-------|--------------|--------------------------------|--------------------|----------------|-----------|---|
| 1     | $f_{op}$     | Frequency of operation         | 0                  | $f_{BUS}/4$    | Hz        | $f_{BUS}$ is the bus clock as defined in <a href="#">Control timing</a> . |
| 2     | $t_{SPSCK}$  | SPSCK period                   | $4 \times t_{BUS}$ | —              | ns        | $t_{BUS} = 1/f_{BUS}$   |
| 3     | $t_{Lead}$   | Enable lead time               | 1                  | —              | $t_{BUS}$ | —   |
| 4     | $t_{Lag}$    | Enable lag time                | 1                  | —              | $t_{BUS}$ | —   |
| 5     | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{BUS} - 30$     | —              | ns        | —   |
| 6     | $t_{SU}$     | Data setup time (inputs)       | 15                 | —              | ns        | —   |
| 7     | $t_{HI}$     | Data hold time (inputs)        | 25                 | —              | ns        | —   |
| 8     | $t_a$        | Slave access time              | —                  | $t_{BUS}$      | ns        | Time to data active from high-impedance state                             |
| 9     | $t_{dis}$    | Slave MISO disable time        | —                  | $t_{BUS}$      | ns        | Hold time to high-impedance state   |
| 10    | $t_v$        | Data valid (after SPSCK edge)  | —                  | 25             | ns        | —   |
| 11    | $t_{HO}$     | Data hold time (outputs)       | 0                  | —              | ns        | —   |
| 12    | $t_{RI}$     | Rise time input                | —                  | $t_{BUS} - 25$ | ns        | —   |
|       | $t_{FI}$     | Fall time input                |                    |                |           |   |
| 13    | $t_{RO}$     | Rise time output               | —                  | 25             | ns        | —   |
|       | $t_{FO}$     | Fall time output               |                    |                |           |   |



NOTE: Not defined

**Figure 19. SPI slave mode timing (CPHA = 0)**

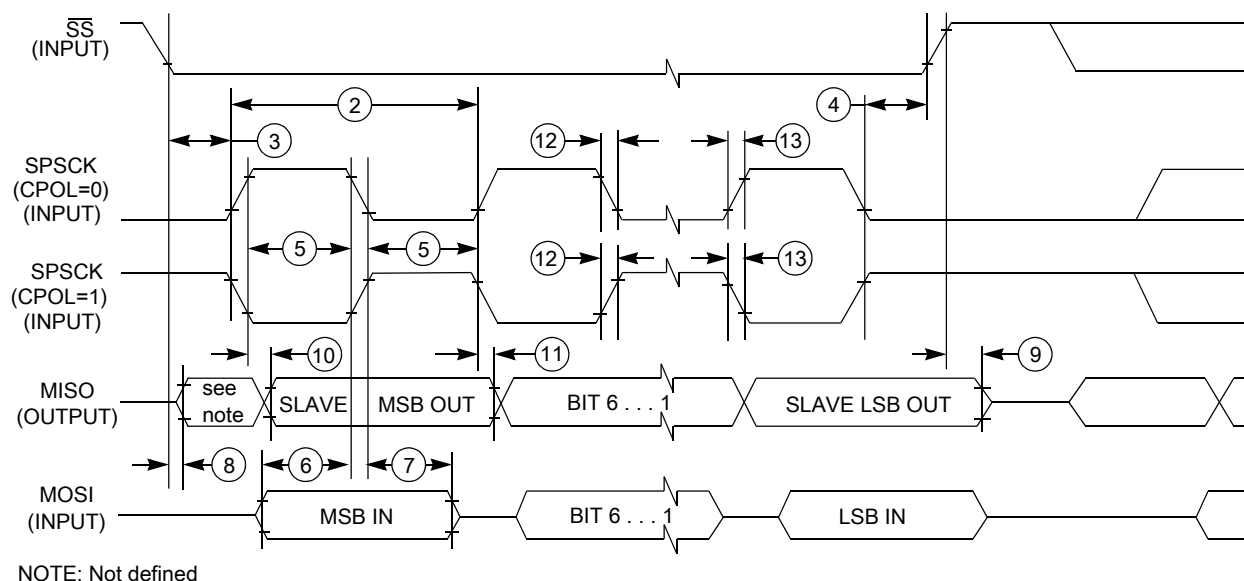


Figure 20. SPI slave mode timing (CPHA=1)

### 5.5.2 MSCAN

Table 16. MSCAN wake-up pulse characteristics

| Parameter                            | Symbol    | Min | Typ | Max | Unit          |
|--------------------------------------|-----------|-----|-----|-----|---------------|
| MSCAN wakeup dominant pulse filtered | $t_{WUP}$ | -   | -   | 1.5 | $\mu\text{s}$ |
| MSCAN wakeup dominant pulse pass     | $t_{WUP}$ | 5   | -   | -   | $\mu\text{s}$ |

## 6 Dimensions

### 6.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to [freescale.com](http://freescale.com) and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|--|-------------------------------|
| 64-pin LQFP                              | 98ASS23234W                   |
| 80-pin LQFP                              | 98ASS23237W                   |

## 7 Pinout

### 7.1 Signal multiplexing and pin assignments

For the pin muxing details see section Signal Multiplexing and Signal Descriptions of KEA128 Reference Manual.

## 8 Revision History

The following table provides a revision history for this document.

**Table 17. Revision History**

| Rev. No. | Date          | Substantial Changes   |
|----------|---------------|---|
| Rev. 1   | 11 March 2014 | Initial Release   |
| Rev. 2   | 18 June 2014  | <ul style="list-style-type: none"> <li>Parameter Classification section is removed.</li> <li>Classification column is removed from all the tables in the document.</li> <li>New section added - <a href="#">Supply current characteristics</a>.</li> </ul>  |
| Rev. 3   | 18 July 2014  | <ul style="list-style-type: none"> <li>Added supported part numbers.</li> <li><a href="#">ESD handling ratings</a> section is updated.</li> <li>Figures in <a href="#">DC characteristics</a> section are updated.</li> <li>Specs updated in following tables:                             <ul style="list-style-type: none"> <li><a href="#">Table 9</a>.</li> </ul> </li> </ul> |
| Rev. 4   | 03 Sept 2014  | <ul style="list-style-type: none"> <li>Data Sheet type changed to "Technical Data".</li> </ul>  |

**How to Reach Us:**

**Home Page:**

[freescale.com](http://freescale.com)

**Web Support:**

[freescale.com/support](http://freescale.com/support)

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. Freescale reserves the right to make changes without further notice to any products herein.

Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: [freescale.com/SalesTermsandConditions](http://freescale.com/SalesTermsandConditions).

Freescale, the Freescale logo, and Kinetis are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. All other product or service names are the property of their respective owners. ARM and Cortex-M0+ are the registered trademarks of ARM Limited.

©2014 Freescale Semiconductor, Inc.